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March 14, 1995

Advanced Research Projects Agency (ARPA)
Contracts Management Office (CMO)
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Arlington, VA 22203-1714

Attention: Mr. Douglas M. Pollock

Subject: Contract No. MDA972-93-C-0057; GTEL Project No. 852
Quarterly Technical Report (SLIN 0002AB)

Dear Mr. Pollock:

GTE Laboratories Incorporated hereby submits the subject report covering the period November 23, 1994 through February 23, 1995, in accordance with the terms of the Contract.

If you should have any questions or require any additional information or further clarification, please contact me at (617)466-2954.

Sincerely,

Deidre B. Ryan

Deidre B. Ryan
Contracts Manager

Enclosure

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During the sixth quarter of the CORD project, Stanford University has continued experimental investigation of the CORD testbed. The transmission and reception of the 2.488 GHz payload data clock and its affect on the payload data and control channels were investigated. The electronic multiplexer and demultiplexer circuits were tested and measured. The payload data pseudo random data generator and bit error rate measurement logic were designed, components selected, and the CRO controller was designed.

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METHODS AND COMPONENTS FOR OPTICAL CONTENTION RESOLUTION IN HIGH SPEED NETWORKS

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Submitted by:

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1. CONSORTIUM EXECUTIVE SUMMARY

During the sixth quarter of the CORD project, Stanford University has continued experimental investigation of the CORD testbed; the contention resolution optics (CRO) was not investigated as it has just been delivered by GTE. The transmission and reception of the 2.488 GHz payload data clock and its affect on the payload data and control channels were investigated. The electronic multiplexer and demultiplexer circuits were tested and measured. The payload data pseudo random data generator and bit error rate measurement logic were designed, components selected and the CRO controller was designed.

The results obtained from our experiments with the multiplexing and demultiplexing portions of the electronic logic have led us to re-design portions of the remaining control logic. This has somewhat delayed the fabrication of our 311 MHz ECL logic printed circuit boards (PCB). We have already implemented our design changes in our schematics and are now performing layout design for the PCB.

We have completed the design for the 2.488 Gbps payload data pseudo-random data generator and bit error checker. When combined, these systems will provide us with the first bit error tester (BER) which works with packet data from multiple sources. Our unique design provides accurate BER testing without secondary control signals between the generator and receiver/error checker. We could, therefore, use our system to test optical packet switched networks with geographically separated transmitters and receivers. Because our BER system works with data from multiple sources, it can be scaled to test metropolitan or wide area networks with several hundred nodes.

The CRO pre-prototype will initially contain a single delay-line module. We have taken this into account and designed a CRO controller for optimum performance in this configuration.

We investigate, theoretically and experimentally, embedded clock transport for the 2.5 Gbps payload data clock transport. A thorough analysis, which includes the phase jittering distribution due to the receiver noise, BER due to phase jittering, and the crosstalk between the payload data and the clock signal has been completed. The non-Gaussian distributed phase jittering results in significant BER floor for smaller clock to noise ratio. Experimental results on the variance of the phase jitter match fairly to the theoretical prediction (within 1 dB). The optical power penalty due to the transport of clock signal versus clock filter bandwidth is been investigated.

Design of the clock filter has been also investigated. The clock recovery time depends on the impulse response of the clock filter and is inversely proportional to the bandwidth of the clock filter. The tradeoff in design between the optical power penalty and the clock recovery time depends upon the clock filter bandwidth. Our experimental results agree very well with our theoretical calculations. For the clock filter with 75 MHz noise bandwidth used in the CORD experiment, the clock recovery time is about 40-50 bits (20 ns), which is less than 10% of the packet duration (250 ns).

During the past quarter the University of Massachusetts group has completed the following tasks:

1. Completion of analysis of ring networks making use of optical Switched Delay Lines (SDL).

2. Implementation of software modules necessary to emulate reconfigurable optical devices in the optical simulator.

3. Preliminary analysis of network architectures making use of the CRO device for performance improvement.

The application of SDL to WDM star networks is well known at this stage of the project and provides a considerable reduction in packet retransmission probability due to receiver contention. The limitation of this approach is in the need to assign each node a specific and unique wavelength for transmission (to allow each node to randomly access the network without generating collision among packets at the hub). This requirement implies that the number of nodes, N, cannot be larger than the number of available wavelengths, w. To circumvent this scalability limitation, we proposed and analyzed a ring topology. The advantage of the ring over the star is that in the ring any node can easily monitor the local traffic within the network so that collisions can be avoided without assigning each node a unique wavelength. The description and the related performance analysis of 3 ring network configurations, namely one with N=w, one with N=2w and one with N=3w, can be found in the complete University of Massachusetts quarterly report issued in February 1995.

During the past three months, the optical simulator under development at University of Massachusetts has been upgraded with the software modules necessary to simulate the behavior of optically reconfigurable devices, such as photonic switches. In addition, the optical receiver software module has been completed to include the necessary data structures to describe the receiver sensitivity, the receiver wavelength, its bandwidth and its status (on/off). This part is essential to evaluate possible network degradation due to noise accumulation within the network, or erroneous wavelength assignment. University of Massachusetts team is currently implementing routines that will model the logical functions of wavelength sensitive devices, such as tunable receivers and AOTF filters. These routines are expected to be completed within the next quarter when University of Massachusetts expects to finish the implementation of the software modules required to simulate the logical functions of wavelength sensitive devices. Once completed, the simulator will be tested, debugged and used to simulate the CORD testbed under development at Stanford. A preliminary analysis of optical bridge architectures with and without the CRO device will be carried out to assess the performance improvement derived from the use of the CRO.

The following sections contain the technical report of GTE Laboratories only. Stanford University and University of Massachusetts will submit their reports separately.

2. TECHNICAL SUMMARY

2.1 CRO INTEGRATION

Integration of the CRO module has been completed. The unit at this time includes two optical $LiNbO_3$ switches (the third switch degraded in performance in time and was sent back to the manufacturer for replacement), three semiconductor optical amplifiers, monitoring modules and polarization adjustment modules. In addition three delay lines are incorporated, one for the header detector and two for packet delay between switches. The CRO module has been packaged in an enclosure with optical and electrical connections to the outside. It was delivered to Stanford University on the last week of February and optical paths were tested. Two connections degraded during the shipment and will be shortly replaced. At this time testing continue and equipment to operate this unit is being assembled.

Replacement units for the degraded connections are being tested at GTE Laboratories in preparation for shipment to Stanford.

The third $LiNbO_3$ switch that is expected to be delivered by GEC Marconi within few weeks, will be evaluated upon receipt, its performance characterized and the unit connectorized for installation in the CRO. The present CRO has been assembled in a manner that permits its operation as a single stage packet switch with an easy upgrade to a dual stage when the last switch is incorporated.

2.2 DIGITAL OPTICAL SWITCH

The digital optical switch is a current injected device where the index of refraction change caused by this current changes the propagation characteristics of the output mode and switches its intensity from one port to another. This operation depends on the waveguides being single mode and hence considerable effort has been devoted to produce well behaved single mode guides needed for good switch performance.

During the last quarter, optical switch test wafers were successfully processed using waveguide dimensions provided by modeling. The waveguides in those wafers were low in ridge height (~1 μm) and narrow in width (3.5 μm). It was demonstrated that higher order vertical or horizontal modes were eliminated in this new design.

These modifications were incorporated into the mask for the packageable switch. In addition, the input waveguide section of the switch was modified to act as a mode stripper by increasing its length to ~1 cm.

A second set of the alignment block and RIE mask plates of the new mask set have been received from the vendor. Fabrication of passive switch structures are now being carried out to test the effectiveness of this new design in eliminating the higher order modes in the packageable switch configuration. This configuration includes longer input and output waveguides and port fanout to allow fiber attachment. The results of these tests will be used in optimizing the design of the rest of the mask plates.

We suffered a two-week delay when the first sets of mask plates were delivered in unusable condition due to a bug in the software that fractures the design data and transmits it to the

mask vendor. The vendor of the commercial software is now taking action to prevent this problem from occurring again.

Due to EPI products delays in supplying wafers, we acquired a second source, Sumitomo, and ordered four switch wafers from them. Unfortunately, the devastating earthquake in Kobe has interrupted our product's run and they are now unable to supply us with any material for four months. The same order has now been placed with EPI products and hopefully by mid March we will receive some of it, if not all.

Our plan to fabricate packageable switches by the end of April, '95 is still in effect, assuming that there are no further delays in obtaining wafers and the rest of the mask plates. As soon as we fabricate the devices, we would be able to characterize them in time to fulfill the April, '95 milestone.

3 MILESTONES

1. Fabrication of a digital optical switch with extinction ratio >20 dB.	Delayed April 1995
2. Optimization of switch design for high speed operation.	Delayed April 1995
3. Construction of CRO pre-prototype.	Completed
4. Testing of CRO pre-prototype.	Completed

The first two milestones have been delayed as explained in the text with completion expected in April 1995.

Milestones 3 and 4 have been completed.